**EE091 ELECTRONIC DEVICES**

**LAB 7**

FET AMPLIFIER

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1. **OBJECTIVES**

This lab introduces the operation of common source and common collector amplifier. You will know how to build a CE, CS circuits, measure the gain and compare to the theory calculation.

# MATERIAL AND EQUIPMENT

* 1. Oscilloscope
  2. Power Supply
  3. Multimeter
  4. CD4007
  5. Assorted Resistors
  6. Assorted Capacitors

# THEORY

Before coming to the laboratory, student must review the definitions of threshold voltage VT, device transconductance parameter 𝑘 , body effect coefficient 𝛾 and channel length modulation coefficient parameter 𝜆.

Depending on the applied DC bias, MOSFETs have thre regions of operation:

* Cutoff region: ID = 0

NMOS: VGS ≤ VTN­

PMOS: VSG ≤ VTP­

* Triode (linear) region:

NMOS: VDS < VOV → ID =

PMOS: VSD < VOV → ID =

* Saturatuon region: ID\_sat. Neglecting the channel length modulation effect.

NMOS: VDS > VOV → ID\_sat = (S1)

PMOS: VSD > VOV → ID\_sat = (S2)

## Threshold voltage (𝑽𝑻)

he voltage at which the surface inversion layer just forms is called threshold voltage (𝑉𝑇). The inversion layer region is an extremely shallow layer, existing as a charge sheet directly below the gate. AT 𝑉𝐺 exceeds the threshold voltage 𝑉𝑇𝑁, the surface has inverted from the p-type polarity of original substrate to an n-type. For the enhance-mode, 𝑉𝑇𝑁 > 0 𝑎𝑛𝑑 𝑉𝑇𝑃 < 0.

## Transconductance parameters

𝑘 𝑎𝑛𝑑 𝑘′ are called transconductance parameters, both have units of 𝐴/𝑉2. The 𝑘 can be estimated as the slope of √𝐼𝐷 from equation (S1) or equation (S2).

## Body effect coefficient 𝜸

When a non-zero substrate bias voltage (𝑉𝑆𝐵) are applied. It has a huge effect on the threshold voltage, thus introduce the body effect coefficiet 𝜸, which can be found from:

|  |  |
| --- | --- |
| 𝑉𝑇 −𝑉𝑇0  𝛾 =  √|2𝜙𝐹| + 𝑉𝑆𝐵 − √|2𝜙𝐹| | (G1) |

Where 𝑉𝑇: threshold voltage when a non-zero 𝑉𝑆𝐵 is applied. 𝑉𝑇0: threshold voltage when 𝑉𝑆𝐵 = 0 𝑉, 𝜙𝐹: substrate Fermi potential.

Note that the substrate bias coefficient is positive in NMOS and negative in PMOS.

## Channel length modulation coefficient parameter

Without neglecting the channel length modulation effect. The Equation(S1) or Equation (S2) can be expained as follows:

|  |  |
| --- | --- |
| 𝐼𝐷\_𝑠𝑎𝑡 = 𝑘 (𝑉𝐺𝑆 − 𝑉𝑇0)2 ∙ (1 + 𝜆 ∙ |𝑉𝐷𝑆|)  2 | (S3) |

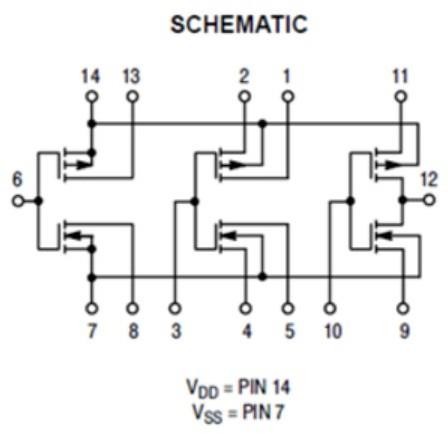
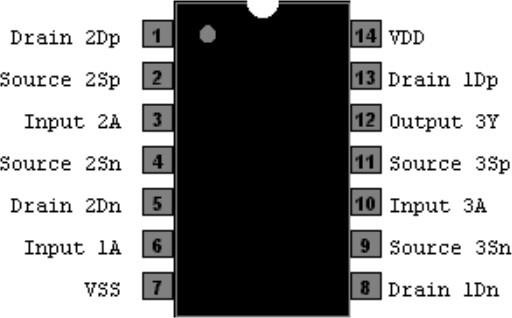
The experiment mesurement of the 𝜆 requires different test circuit setup. The 𝑉𝐺𝑆 is set to

𝑉𝑇0 + 1. The 𝑉𝐷𝑆 is chosen sufficiently large so that the transistor operates in the saturation mode. The 𝐼𝐷\_𝑠𝑎𝑡 is measured for two different drain voltage values, 𝑉𝐷𝑆1𝑎𝑛𝑑 𝑉𝐷𝑆2. Since the 𝑉𝐺𝑆 = 𝑉𝑇0 + 1, the ratio of the measured drain current values I𝐷1 𝑎𝑛𝑑 𝐼𝐷2 is:

|  |  |
| --- | --- |
| 𝐼𝐷2 = 1 + 𝜆 ∙ 𝑉𝐷𝑆2  𝐼𝐷1 1 + 𝜆 ∙ 𝑉𝐷𝑆1 | (S4) |

# CD4007 pinout

CD4007 is comprised of three n-channel and three p-channel enhancement MOS transistors. The pinout of CD4007 is shown in Fig.1.



# PROCEDURE

## Common-Source Amplifier

The basic common-source (CS) circuit is shown in Figure 1. In comparison to the BJT common-emitter amplifier, the FET amplifier has a much higher input impedance, but a lower voltage gain. The voltage gain of the circuit can be expressed as:

Av = -gmRD

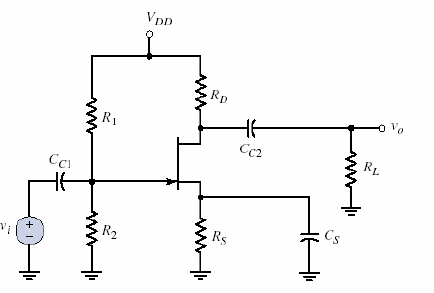


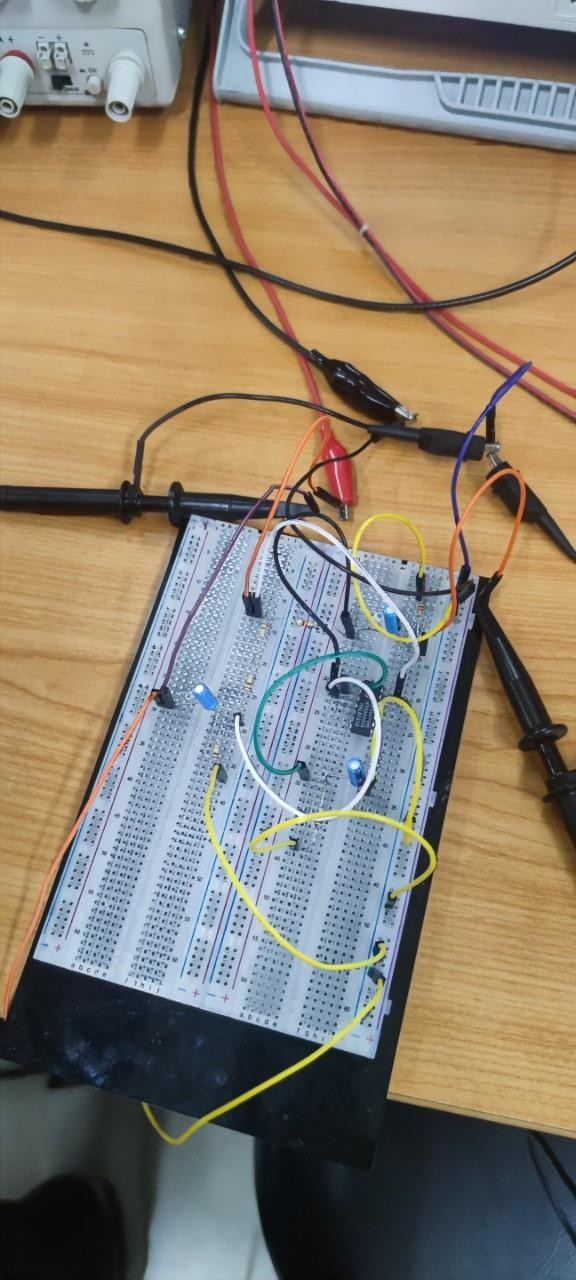
Figure 1

Connect the circuit as shown in Figure 1.

Use Cc1 = 0.1μF, Cc2 = 1μF, Cs = 0.1 μF, RS = 1kΩ, RD = 47 kΩ, R1 = 200kΩ, R2=100 kΩ, VDD = 12V.

A diagram of a circuit

Description automatically generated



Apply a sinusoidal signal with frequency 1kHz, amplitude 0.4Vp-p

1. Observe the output.
2. Capture both input and output waveforms.
3. Calculate the voltage gain.
4. Perform a frequency sweeping from 1Hz to 100KHz. Plot the frequency response of voltage gain (𝑉𝑜) dB.

𝑉

𝑖

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Frequency | Gain | Frequency | Gain | Frequency | Gain | Frequency | Gain |
| 100 | 0.049 | 1000 | 0.0421 | 10,000 | 0.034 | 60,000 | 0.04138 |
| 200 | 0.043 | 2000 | 0.0406 | 20,000 | 0.042 | 70,000 | 0.0414 |
| 400 | 0.042 | 3000 | 0.04060 | 30,000 | 0.039 | 80,000 | 0.04135 |

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 600 | 0.0403 | 4000 | 0.039 | 40,000 | 0.04 | 90,000 | 0.034 |
| 800 | 0.0412 | 5000 | 0.03971 | 50,000 | 0.0387 | 100,000 | 0.041 |

1. Connect Cc2 = 1μF to the Drain terminal. Capture the waveforms and measure the gain. Then, connect the load resistor RL =1 kΩ, one pin is connected to the capacitor

Cc2, the other pin is connected to the ground. Perform a parameter sweep on RL from 1 KOhm to 100 Kohm. observe the effects of *R*4 on the Vout of the circuit, and

comment on results. Assume that Vin does not change, compute the gains [𝑣𝑜𝑢𝑡] 𝑑𝐵

𝑣𝑖𝑛

based on the change the value of *RL* .

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 𝑅𝐿 | Gain  (Simulation) | Gain  (Measurement) | 𝑅𝐿 | Gain  (Simulation) | Gain  (Measurement) |
| 1𝑘Ω | 0.039 | 0.0432 | 5.6𝑘Ω | 0.132 | 0.123 |
| 2.2𝑘Ω | 0.0612 | 0.0614 | 6.8𝑘Ω | 0.112 | 0.141 |
| 3.3𝑘Ω | 0.08 | 0.0812 | 10𝑘Ω | 0.134 | 0.15 |
| 4.7𝑘Ω | 0.111 | 0.1054 | 100𝑘Ω | 0.112 | 0.158 |